SESSION 5 – TAPA II
Advanced Transistor Technology I

Tuesday, June 15, 1:30 p.m.
Chairpersons: K. DeMeyer
K. Shibahara, Hiroshima University

5.1 — 1:30 p.m.
Fully Working 1.10μm^2 Embedded 6T-SRAM Technology with High-k Gate Dielectric Device for Ultra Low Power Applications, H.-J. Ryu, W.-Y. Chung, Y.-J. Jang, Y.-J. Lee, H.-S. Jung, C.-B. Oh, H.-S. Kang and Y.-W. Kim, Samsung Electronics Co., Ltd., Kyonggi-Do, Korea

Ultra low power 1.10um2 6T-SRAM chip with HfO2-Al2O3 (EOT=17A) was successfully demonstrated. By carefully optimizing gate pre-doping process, device performance was improved. The threshold voltage was well controlled to acceptable value by channel engineering. Current performance of NFET and PFET were 335 and 115uA/um (Ioff=0.9/2.0pA/um). Stand-by current of SRAM chips with HfO2-Al2O3 was decreased by 2 orders, while access time was 1.65 times larger compared with that of SRAM chips with oxynitride at Vdd=1.2V.

5.2 — 1:55 p.m.
A 65nm-node LSTP (Low Standby Power) Poly-Si/a-Si/HfSiON Transistor with High I_{on}-$I_{standby}$ Ratio and Reliability, Y. Yasuda, N. Kimizuka, T. Iwamoto*, S. Fujieda*, T. Ogura*, H. Watanabe*, T. Tatsumi*, I. Yamamoto, K. Ito, H. Watanabe*, Y. Yamagata and K. Imai, NEC Electronics Corporation, Kanagawa, Japan, *NEC Corporation, Kanagawa, Japan

We have newly developed Poly/a-Si/HfSiON Transistor that features high Ion-I standby ratio and reliability for 65nm-node LSTP (Low Standby Power) application. By carefully optimizing pocket implant condition, excellent Ion-Istandby (=Ig+Ioff) characteristics of Ion=520uA/Istandby=17pA at Vdd=1.2V are obtained, which is the highest ratio ever reported. In addition, we have newly introduced thin amorphous-Si layer between HfSiON and phosphorous-doped Poly-Si gate-electrode for reliability enhancement, and confirmed that PBTI lifetime improves by two orders of magnitude with no performance degradation.

5.3 — 2:20 p.m.
55nm High Mobility SiGe(:C) pMOSFETs with HfO_2 Gate Dielectric and TiN Metal Gate for Advanced CMOS, O. Weber, F. Ducroquet, T. Ernst, F. Andrieu, J.-F. Damlencourt, J.-M. Hartmann, B. Guillaumot*, A.-M. Papon, H. Dansas, L. Brévard, A. Toffoli, P. Besson*, F. Martin, Y. Morand* and S. Deleonibus, CEA/DRT-LETI, Grenoble Cedex, France, *STMicroelectronics, Crolles Cedex, France

For the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gatelength. SiGe(:C) surface channel pMOSFETs with HfO2 gate dielectric exhibit a 10000 gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO2/Si reference. With such a thin Equivalent Oxide Thickness (EOT=16-18Å), this represents the best gate leakage/mobility trade-off ever published.

5.4 — 2:45 p.m.
Systematic Study of pFET V_t with Hf-Based Gate Stacks with Poly-Si and FUSI Gates, E. Cartier, V. Narayanan, E. P. Gusev, P. Jamison, B. Linder, M. Steen, K. K. Chan, M. Frank, N. Bojarczuk, M. Copel, S. A. Cohen, A. Callegari, S. Zafar, M. Gribelyuk*, M. Chudzik, C. Cabral Jr., R. A. Carruthers , C. D?Emic, J. Newbury, D. Lacey, S. Guha and R. Jammy, IBM SRDC, Yorktown Heights, NY and *IBM Microelectronics Division, Hopewell Junction, NY

It is shown that the large Vfb/Vt shifts in pFETs with Hf-based dielectrics are set during poly-Si deposition and do not change during subsequent processing, identifying the low temperature reaction between Si and Hf-based dielectrics as the root cause for the shifts. The reaction could not be prevented by engineering closed cap-layers (Si3N4, Al2O3), and large shifts were observed even after full gate silicidation (FUSI). Some improvements were observed with ultra thin Si-rich Hf-silicate layers.